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INFORMATION DISCLOSURE STATEMENT *#1*

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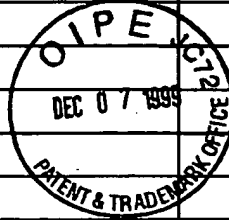
Applicant: Shunpei YAMAZAKI et al.

Filing Date: April 8, 1999

Group: 2871

U.S. PATENT DOCUMENTS

Examiner Initial	Patent Number	Issue Date	Patentee	Class	Subclass	Filing Date (if approp.)
<i>Q</i>	5,144,392	09/01/92	Brotherton			
<i>Q</i>	4,930,874	06/05/90	Mitsumune et al.			



FOREIGN PATENT DOCUMENTS

	Document Number	Date	Country	Class	Subclass	Translation	
						Yes	No
<i>Q</i>	56-81972	07/04/81	Japan			Abst.	
<i>Q</i>	58-32466	02/25/83	Japan			Abst.	
<i>Q</i>	58-124273	07/23/83	Japan			Abst.	
<i>Q</i>	58-158967 <i>NY</i>	09/21/83	Japan			Abst.	
<i>Q</i>	58-115864	07/09/83	Japan			Abst.	
<i>Q</i>	59-214262	12/04/84	Japan			Abst.	
<i>Q</i>	62-124769	06/06/87	Japan			Abst.	
<i>Q</i>	1-161316	06/26/89	Japan			Abst.	

OTHER DOCUMENTS (Including Author, Title, Relevant Pages, Date, Place of Publication)

<i>Q</i>	Wolf et al., Silicon Processing for the VLSI ERA, Lattice Press, Volume 1, 1989, pages 151-154
<i>Q</i>	Wolf et al., Silicon Processing for the VLSI ERA, Lattice Press, Volume 2, pages 66-72
Examiner <i>Q</i>	Date Considered <i>12/6/00</i> <i>12/14/06</i>

*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.